TRUESTREAM

Slow FIR filter

FIR filters are one of the most common components for signal processing in an FPGA. However in many applications the data sample rate is significantly lower than the FPGA clock speed, which means that full throughput is not necessary. This is what we call a ”slow FIR filter”. In this scenario we can use a more optimized FIR filter implementation which utilizes only a single DSP element to serve one or more non-synchronous channels. Since resource utilization is often critical in FPGA projects, Truestream has developed a very efficient IP for this operation.

Key features

- Uses only one DSP element and minimal LUT/FF.
- Supports multiple channels, independent from each other.
- Handshake interface (ready/valid) for data bus on input and output side.
- Optimized modes for interpolation and decimation.

Format

- Written in VHDL-2008. Can be used in any design targeting any vendor.
- Delivery contains human-readable source code, testbenches, and technical documentation.

Resource utilization

The design is highly area optimized, while remaining portable. Below is a comparison with a competitor’s slow FIR filter implementation, when targeting a Xilinx 7-series device. All the examples use 255 coefficients and a data width of 25 bits.

One channel		
	Truestream	Competitor
LUT	74	107
FF	70	166
BRAM36	0.5	1
DSP	1	1

Four channels		
	Truestream	Competitor
LUT	139	428
FF	91	664
BRAM36	1	4
DSP	1	4

Four channels, interpolation by four		
	Truestream	Competitor
LUT	104	684
FF	82	924
BRAM36	0.5	2
DSP	1	4

Four channels, decimation by four		
	Truestream	Competitor
LUT	141	468
FF	93	676
BRAM36	1	4
DSP	1	4

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