TRUESTREAM

AXI master

An AXI master is a convenient tool for performing memory read/write operations from your FPGA design. It handles the complexity of raw AXI transactions and instead presents a very simple interface to the user. This type of tool is also referred to as a "data mover" or "AXI MM2S/S2MM". Since resource utilization is often critical in FPGA projects, Truestream has developed a very efficient IP for this operation. It provides optimal bus utilization at only a fraction of the logic footprint, so that you can get even more out of your design.

Key features

- Compliant with the AXI4 and AXI3 standards.
- Achieves 100% utilization of the data channels (R and W) without overhead.
- Intuitive interface that is easy to use.
- Very portable and parameterizable.
- Very small logic footprint.

Format

- Written in VHDL-2008. Can be used in any design targeting any vendor.
- Delivery contains human-readable source code, testbenches, and technical documentation.

Resource utilization

The design is highly area optimized, while remaining portable and high performing. Below is a comparison with competing AXI master implementations, when targeting a Xilinx 7-series device. The comparisons are done with data width 64, address width 32 and ID width 8. Asynchronous operation was enabled, data FIFO depth set to 2048 and command FIFO depth set to 16.

AXI read master			
	Truestream	Competitor A	Competitor B
LUT	233	703	988
FF	338	946	468
BRAM36	4	6	4

AXI write master			
	Truestream	Competitor A	Competitor B
LUT	291	1058	1113
FF	405	1359	568
BRAM36	4	5.5	4

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