

# AXI data width converter

A data width converter is a very common component in an AXI subsystem. A typical use case is when many modules share a single physical AXI port, and the different modules use different native data widths. For them to be connected to the physical port they have to be converted to use the width of the physical port.

The width converter manipulates the address channels (AR and AW) to match a specified bus width, and the data channels (R and W) are converted using a gearbox. Since resource utilization is often critical in FPGA projects, Truestream has developed a very efficient IP to perform this operation.

## Key features

- Performs upconversion (narrow to wide bus) or downconversion (wide to narrow bus).
- Follows the AXI4 standard.
- Very small logic footprint.
- Achieves almost full utilization of the data channels. There is a one-cycle overhead for each burst.

## Format

- Written in VHDL-2008. Can be used in any design targeting any vendor.
- Delivery contains human-readable source code, testbenches, and technical documentation.

## Resource utilization

The design is highly area optimized, while remaining portable. Below is a comparison with a competitor's AXI data width converter implementation, when targeting a Xilinx 7-series device.

AXI read conversion, 32 to 64		
	Truestream	Competitor
LUT	99	221
FF	238	364

AXI write conversion, 32 to 64		
	Truestream	Competitor
LUT	106	258
FF	243	307

AXI read conversion, 64 to 32		
	Truestream	Competitor
LUT	179	378
FF	374	465

AXI write conversion, 64 to 32		
	Truestream	Competitor
LUT	199	431
FF	382	463

---

**Address**

Truestream AB  
Brynhilds gata 7  
583 72 Vikingstad

**Contact**

info@truestream.se  
www.truestream.se

**VAT number**

SE559166520201