TRUESTREAM

AXI4-to-AXI3 converter

An AXI4-to-AXI3 converter is a simple tool that adapts AXI4 transactions to be compliant with the older version of the standard. The AXI3 standard has a shorter maximum burst length and requires a write ID to be set, which enables data interleaving. Since resource utilization is often critical in FPGA projects, Truestream has developed a very efficient IP for this operation.

Key features

- Implements burst splitting, write ID handling, and write response aggregation.
- Maintains 100% utilization of the read/write data channels. Zero cycles wasted when converting.
- Extensively verified with testbenches and automated on-target tests.
- Small logic footprint.

Format

- Written in VHDL-2008. Can be used in any design targeting any vendor.
- Delivery contains human-readable source code, testbenches, and technical documentation.

Resource utilization

The design is highly area optimized, while remaining portable and achieving full throughput. Below are some comparisons with a competitor's conversion implementation, when targeting a Xilinx 7-series device.

With settings: Address width = 28, ID width = 0, data width = 32.

AXI read conversion		
	Truestream	Competitor
LUT	69	138
FF	65	158

AXI write conversion		
	Truestream	Competitor
LUT	108	197
FF	87	227

With settings: Address width = 32, ID width = 8, data width = 128.

AXI read conversion		
	Truestream	Competitor
LUT	73	165
FF	77	191

AXI write conversion		
	Truestream	Competitor
LUT	110	246
FF	115	283

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